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PATNET

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant   :   Weiss et al.
Serial No.   :   09/750,733   Examiner   :
Filed   :   December 27, 2000   Group Art Unit:
For :   METHOD AND APPARATUS FOR PRODUCING INSTRUCTION
          WORDS TO TRIGGER FUNCTIONAL UNITS IN A PROCESSOR

RESPONSE TO NOTICE TO FILE MISSING
PARTS AND PRELIMINARY AMENDMENT

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April 11, 2001
Date of Deposit

| James J. Maune | 26,946 |
| Attorney Name | PTO Registration No |

| | April 11, 2001 |
| Signature | Date of Signature |

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Responsive to the Notice to File Missing Parts, a copy of which is enclosed,

Applicants hereby submit a translation of the original German language application. The

undersigned attorney believes this translation to be accurate.

Also submitted herewith is a Declaration signed by the Inventors.

The required fee of $130 is enclosed.

Preliminary Amendment

Please substitute the attached Substitute Specification, Drawing and Abstract for the Specification, Drawing and Abstract as originally filed and the concurrently filed translation. The Substitute Specification is a revision of the translation to use idiomatic English and to place the specification in a form consistent with U.S. Practice. No new matter is added.

Please cancel Claims 1 to 3.

Add the following Claims:

4. (New)   In a method for operating a processor wherein a sequence of one or more instruction words are derived from a translation of program code, each instruction word having a plurality of instruction word parts, each word part arranged to trigger a functional unit of a processor, and wherein said instruction word parts are formed into program words and said program words are used to form secondary instruction words for operating said processor which are stored in a secondary instruction word memory; the improvement wherein instruction word parts corresponding to data-stationary commands are assembled as complex words in a complex word sequence, identified by a complex word pointer and stored in a complex word table at a location corresponding to said pointer, wherein said complex word pointers are provided as program words corresponding to said data-stationary commands, and wherein upon encountering said complex word pointers in said program words during execution, said complex words are

read from said complex word table and stored in parallel in said secondary instruction word memory.

5.   (New) A method as specified in claim 4 wherein said complex words further include assignments for storage of said complex words in said secondary instruction word memory.

6.   (New) A method as specified in claim 4 wherein said secondary instruction word memory is operated in a fixed sequence.

7.   (New) In a processor wherein program codes are translated into a sequence of instruction words, each having a plurality of instruction word parts, each word part being arranged to trigger a functional unit of a processor, and wherein instruction words are sequentially provided to said processor functional units via a buffer memory, the improvement wherein there is provided a memory for storing instruction word parts corresponding to data-stationary commands, said instruction word parts being stored at a location corresponding to a complex word pointer corresponding to a data-stationary command, and wherein said memory is arranged to transfer said complex word parts to said buffer memory in parallel to execute a data-stationary command.

8.   (New) The improved processor as specified in claim 7 further having an execution memory wherein instruction word sequences are stored in the form of program words , and wherein there is provided a configuration processor for storing said complex word pointers as program words in said execution memory for data-stationary commands
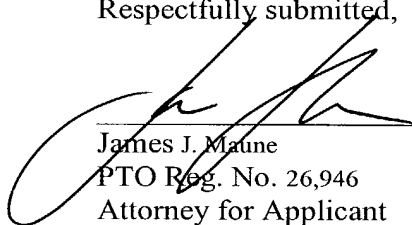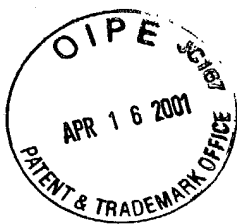
R E M A R K S

Applicants have amended the specification and submit herewith a revised specification in conformance with U.S. Practice.

Claims 1-3 have been cancelled. New Claims 4-8 conform to U.S. Practice and have substantially the same scope.

Respectfully submitted,

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TO ALL WHOM IT MAY CONCERN:

Be it known that WE, MATTHIAS WEISS and GERHARD FETTWEIS, citizens of Germany, residing in Dresden,Germany whose post office addresses are Bernhardstraße 111, 01187 Dresden, Germany; and Plattleite 39, 01324 Dresden, Germany, respectively, have invented an improvement in

METHOD AND APPARATUS FOR PRODUCING INSTRUCTION WORDS TO TRIGGER FUNCTIONAL UNITS IN A PROCESSOR

of which the following is a

SUBSTITUTE SPECIFICATION

BACKGROUND OF THE INVENTION

[0001]   The invention relates to a method of generating instruction words to

trigger functional units in a processor, where, in a configuration phase, a sequence of

primary instruction words deriving from a translation of a program code is generated,

each primary instruction word consisting of several instruction word parts and each

instruction word part is intended to trigger a functional unit of the processor, and the

instruction word part in one or several primary instruction words serves to execute a

data-stationary command. In a known arrangement each primary instruction word may

be compressed and provided as a program word in an execution memory. In an execution phase, secondary instruction words corresponding to the primary instruction words are synthesized out of the stored program words.

[0002]   The invention relates further to an apparatus for producing instruction words to trigger functional units in a processor having functional units, having an instruction word memory associated with said functional units, and having an instruction word buffer for storing instruction words already generated with a latitude at least equal to the bit latitude of the secondary instruction word, the instruction word buffer consisting of a memory having alternative or fixedly programmed line access.

[0003]   In German Patent DE 198 59 389 C1, a method and an apparatus for triggering functional units in a processor are described. By this method and the associated apparatus, while retaining a small program word latitude, the working speed is application-specifically enhanced.

[0004]   The inventors have realized that further enhancement in working speed is possible because some of the commands are data-stationary. Data-stationary means, in this case, that a command affords no definite information on the route by which a processor is to execute the command, in particular the number of steps required to carry out the command.

[0005]   In the execution of a data-stationary command, various steps are carried out in several beats. Each of these steps is carried out by an instruction word part in one instruction word of a sequence of instruction words, each instruction word part prompting

a functional unit of the processor to perform a certain action carrying out a partial step of the execution of the command.

[0006]   Each instruction word, according to the known approach, must be newly composed over the sequence of program words. Even in the case of performing identical commands, it is necessary to generate instruction words corresponding to the partial steps of each command and to compose the program words for this purpose. This is necessary also in the case of identical commands, that is, for like command sequences, new, albeit identical program word sequences are required again and again. This entails a large memory utilization and considerable processing time.

[0007]   It is an object of the invention, then, to reduce the memory utilization and enhance the working speed.

SUMMARY OF THE INVENTION

[0008]   The invention makes it possible to describe the processing of the commands of most frequent occurrence, always performed with the same hardware components and always on the same routes, with the corresponding instruction word parts stored in a complex word sequence. When such a command occurs, the contents of the complex word tables may be consulted to retrieve the instruction word parts for command execution. The special treatment of each recurring command as a normal (variable) command may be eliminated, thereby relieving the program word memory and enhancing the working speed.

[0009]   The invention will be illustrated below in more detail with reference to an

embodiment by way of example.

BRIEF DESCRIPTION OF THE DRAWING

[0010]   The drawing shows an embodiment of complex word processing

according to the invention.

BRIEF DESCRIPTION OF THE PREFERRED EMBODIIMENT

[0011]   In the method of triggering functional units 12 in a processor 13 as

represented in the figure of the drawing, in accordance with the prior art and hence

according to German Patent DE 198 59 389 C1, from a program code 1 by means of a

translation in a configuration phase, a sequence of primary instruction words 2 consisting

of several instruction word parts 4 is generated. Further, the sequence of primary

instruction words 2 is compressed in the program word production 8 and stored as a

sequence of corresponding program words in an execution memory 9.

[0012]   According to a preferred arrangement according to the invention, within

the configuration phase, the instruction word parts 4 serving to execute a data-stationary

command are assembled in a complex word sequence 18 and stored in a line, indicated by

the complex word pointer 6, of the complex word table stored in complex word

memory 5. The complex word pointers 6 are themselves stored in the execution

memory 9.

[0013]   In an execution phase, complex word pointers 6, occurring in the execution memory 9, are recognized and, with the index they contain, specify the line of the complex word table 5 to be read out, which contains the associated complex word sequence 18.

[0014]   The complex word sequence 18 is read out, and the complex words 17 contained in it are transferred in parallel to the corresponding rows and columns of the secondary instruction word memory 7 following assignments internal to the complex words. The complex word table may generated durng the configuration phase of processing or may be a fixed table of complex words that we called by specified pointers corresponding to program commands.

[0015]   Corresponding to the adjusted secondary instruction word memory sequence 16, firstly the current secondary instruction word 15 is transferred into an instruction word output memory 11. Its output triggers the functions required for processing at the corresponding functional units 12 of the processor 13.

[0016]   The current secondary instruction word 15 is also processed in a secondary instruction word production 10 unit together with a new program word, so that at its output, an additional secondary instruction word 15 is placed in readiness for storage in the secondary instruction word memory 7.

WE CLAIM:

1   4.   In a method for operating a processor wherein a sequence of one or

2   instruction words are derived from a translation of program codes, each instruction word

3   having a plurality of instruction word parts, each word part arranged to trigger a

4   functional unit of a processor, and wherein said instruction word parts are formed into

5   program words and said program words are used to form secondary instruction words for

6   operating said processor which are stored in a secondary instruction word memory; the

7   improvement wherein instruction word parts corresponding to data-stationary commands

8   are assembled as complex words in a complex word sequence, identified by a complex

9   word pointer and stored in a complex word table at a location corresponding to said

10   pointer, wherein said complex word pointers are provided as program words

11   corresponding to said data-stationary commands, and wherein upon encountering said

12   complex word pointers in said program words during execution, said complex words are

13   read from said complex word table and stored in parallel in said secondary instruction

14   word memory.

15   5.   A method as specified in claim 1 wherein said complex words

16   further include assignments for storage of said complex words in said secondary

17   instruction word memory.

1   6.   A method as specified in claim 1 wherein said secondary

2   instruction word memory is operated in a fixed sequence.

ABSTRACT OF THE DISCLOSURE

In a digital processor, a reduction of memory utilization and an enhancement of operating speed are achieved in that the instruction word parts of a data-stationary command are assembled in a complex word sequence during a configuration phase and stored in a complex word table. The complex word sequence there deposited is read out, in an execution phase, from the row indicated by a complex word pointer in the complex word table. The complex words contained in it are stored parallelwise by the several assignments internal to the complex words in the corresponding row and column of the secondary instruction word memory, and after output to the corresponding functional units in an instruction word output memory, are able to trigger the required functions.